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EXAMINER	
BLACKMAN, ANTHONY J	

ART UNIT	PAPER NUMBER
2676	17

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/423,415	MORIOKA, SEISUKE	
	Examiner	Art Unit	
	ANTHONY J BLACKMAN	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) *11-20 and 22-34* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-20 and 22-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *14 OCTOBER 2003*.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, see Paper No. 14, Request for Reconsideration filed 6/13/03, with respect to Applicant establishing the filing date of may 7, 1997 of Japanese priority application JP-116772 enclosing a certified translation of JP-116772, disqualifies the supporting reference DYE et al, US Patent Publication no. 20020158865 modified VAN HOOK et al, US Patent No. 6,166,748, have been fully considered and are persuasive. The previous office action of Paper No. 14 has been withdrawn.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 11-20 and 22-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over BUCKELEW et al, US Patent No. 6,667,744 in view of VAINSENCHER, US Patent No. 5,977,997.

4. As per claim 14, examiner interprets BUCKELEW et al to suggest an apparatus for image processing (figure 1, including elements 124-graphics engine integrated into a

single chip (integrate a texture processor and graphics engine) and element 110-a set of dual resolver chips combine to bear similar results to a graphics engine contained within a single chip, including electrically coupled components 114-texture buffer and 116-frame buffer),

comprising: a processor (figure 1, elements 124-graphics engine integrated into a single chip (integration of a texture processor and graphics engine bear similar results to a processor as claimed) and element 110-a set of dual resolver chips combine to bear similar results to a graphics engine contained within a single chip combine to bear similar results to a processor means);

a first storage device (figure 1, element 114-buffer memory) having texture data and electronically coupled to said processor (figure 1, elements 124 and 110 combined bear similar results to said processor);

a texture buffer (figure 1, element 114) coupled to said processor (shown above), transmission of texture data between [said] texture buffer electrically coupled to said processor is faster than transmission of texture data between said storage device and said processor (figure 1 elements 124, 126 transmit data more quickly to texture memory-element 114 than element 124 transmits data to first element 110-the dual set of resolvers that then transmits data less quickly than to the buffer memory-element 116, further column 5, lines 45-56 fully explain said limitation as claimed)however, the processor does not expressly teach inclusion of a data decompression circuit.

Examiner interprets VAINSENCHER to at least suggest a processor

including a data decompression circuit (figure 2, column 4, line 54-column 5, line 14, please note element 206-MPEG Coprocessor for decompression means). It would have been obvious to one skilled in the art at the time of the invention to utilize **multimedia computer chip system 200** of figure 2 as a processor including the MPEG Coprocessor of decompression means with the graphic engine means

(figure 1, including elements 124-graphics engine integrated into a single chip (integrate a texture processor and graphics engine) and element 110-a set of dual resolver chips combine to bear similar results to a graphics engine contained within a single chip, including electrically coupled components 114-texture buffer and 116-frame buffer)

of BUCKELEW et al because both inventions were designed for single chip computer systems. **Advantages of single chip computer systems** by VAINSECHER are at least as follows, "..highly integrated, single chip computer system (abstract, line 1), as well as adding a further advantage of "[T]he single chip computer system is particularly suitable for video game consoles having high quality graphics and/or video, digital video disk (DVD) players and set-top boxes (abstract, lines 14-16)".

Therefore, it would have been obvious to modify BUCKELEW et al by VAINSENCHER because both inventions share similar technological environments corresponding to graphics and video processings in single chip computer systems.

5. As per claim 15, the recited claim limitations bear similar results to claim 14 in addition to the following recited claim features further limiting claim 14; **a first data bus** and **a second data bus**, wherein said **first data bus** carries texture data between said texture buffer and said processor and said processor faster than said **second data bus** carries texture data from said storage device and said processor. The first data bus shown in figure 1 as element 126 and the second data bus s shown as element 120 (second data bus) connecting elements 124 and the combination of elements 110-set of dual resolvers with 116-buffer memory.

6. As per claim 23, BUCKELEW et al disclose an image processing method processing (figure 1, including elements 124-graphics engine integrated into a single chip (integrate a texture processor and graphics engine) and element 110-a set of dual resolver chips combine to bear similar results to a graphics engine contained within a single chip, including electrically coupled components 114-texture buffer and 116-frame buffer)

comprising the steps of: providing a processor (figure 1, elements 124-graphics engine integrated into a single chip (integration of a texture processor and graphics engine bear similar results to a processor as claimed) and element 110-a set of dual resolver chips combine to bear similar results to a graphics engine contained within a single chip combine to bear similar results to a processor means);

and transferring the data between said texture buffer and said processor faster than transferring data between said storage device and said processor (figure 1 elements

124, 126 transmit data more quickly to texture memory-element 114 than element 124 transmits data to first element 110-the dual set of resolvers that then transmits data less quickly than to the buffer memory-element 116, further column 5, lines 45-56 fully explain said limitation as claimed)

however,

does not explicitly teach providing compressed texture data in a storage device; reading said compressed texture data from said storage device and decompressing said compressed texture data in a texture buffer; and storing said decompressed texture data in texture buffer.

Examiner interprets VAINSENCHER to providing compressed texture data in a storage device Examiner interprets VAINSENCHER to at least suggest a processor including a data decompression circuit (figure 2, column 4, line 54-column 5, line 14, please note element 206-MPEG Coprocessor for decompression/compression means); reading said compressed texture data from said storage device and decompressing said compressed texture data in a texture buffer (figure 2, column 4, line 54-column 5, line 14, please note element 206-MPEG Coprocessor for decompression/compression means); and storing said decompressed texture data in texture buffer (figure 2, column 4, line 54-column 5, line 14, please note element 206-MPEG Coprocessor for decompression means).

It would have been obvious to one skilled in the art at the time of the invention to utilize **multimedia computer chip system 200** of figure 2 as a processor including

the MPEG Coprocessor of decompression means with the graphic engine means

(figure 1, including elements 124-graphics engine integrated into a single chip (integrate a texture processor and graphics engine) and element 110-a set of dual resolver chips combine to bear similar results to a graphics engine contained within a single chip, including electrically coupled components 114-texture buffer and 116-frame buffer)

of BUCKELEW et al because both inventions were designed for single chip computer systems. **Advantages of single chip computer systems** by VAINSECHER are at least as follows, "..highly integrated, single chip computer system (abstract, line 1), as well as adding a further advantage of "[T]he single chip computer system is particularly suitable for video game consoles having high quality graphics and/or video, digital video disk (DVD) players and set-top boxes (abstract, lines 14-16)".

Therefore, it would have been obvious to modify BUCKELEW et al by VAINSENCHER because both inventions share similar technological environments corresponding to graphics and video processings in single chip computer systems.

7. As per claim 11, BUCKELEW et al as modified meet limitations for claim 14. BUCKELEW et al also suggest in addition to the following limitation; further comprising a frame buffer (corresponds to the figure 1, element 116-buffer memory), wherein said processor stores image data in said frame buffer (column 2, lines 23-46, 47-64 represent two separate embodiments and column 3, line 62-column 4, line 15).

It would have been obvious to one skilled in the art at the time of the invention to utilize **multimedia computer chip system 200** of figure 2 as a processor including the MPEG Coprocessor of decompression means with the graphic engine means (figure 1, including elements 124-graphics engine integrated into a single chip (integrate a texture processor and graphics engine) and element 110-a set of dual resolver chips combine to bear similar results to a graphics engine contained within a single chip, including electrically coupled components 114-texture buffer and 116-frame buffer) of BUCKELEW et al because both inventions were designed for single chip computer systems. **Advantages of single chip computer systems** by VAINSECHER are at least as follows, "..highly integrated, single chip computer system.(abstract, line 1), as well as adding a further advantage of"..[T]he single chip computer system is particularly suitable for video game consoles having high quality graphics and/or video, digital video disk (DVD) players and set-top boxes (abstract, lines 14-16)". Therefore, it would have been obvious to modify BUCKELEW et al by VAINSENCHER because both inventions share similar technological environments corresponding to graphics and video processings in single chip computer systems.

8. As per claim 12. BUCKELEW et al as modified meet limitations for claim 14, however, BUCKELEW et al does not explicitly teach the limitation of claim 12. VAINSENCHER suggest, "..wherein said processor reads decompressed texture data

contained in said texture buffer and performs image processing of said decompressed texture data for conversion to image data (figure 2, column 4, line 54-column 5, line 14, please note element 206-MPEG Coprocessor for decompression/compression means); reading said compressed texture data from said storage device and decompressing said compressed texture data in a texture buffer (figure 2, column 4, line 54-column 5, line 14, please note element 206-MPEG Coprocessor for decompression/compression means)".

It would have been obvious to one skilled in the art at the time of the invention to utilize **multimedia computer chip system 200** of figure 2 as a processor including the MPEG Coprocessor of decompression means with the graphic engine means (figure 1, including elements 124-graphics engine integrated into a single chip (integrate a texture processor and graphics engine) and element 110-a set of dual resolver chips combine to bear similar results to a graphics engine contained within a single chip, including electrically coupled components 114-texture buffer and 116-frame buffer) of BUCKELEW et al because both inventions were designed for single chip computer systems. **Advantages of single chip computer systems** by VAINSECHER are at least as follows, "..highly integrated, single chip computer system (abstract, line 1), as well as adding a further advantage of "[T]he single chip computer system is particularly suitable for video game consoles having high quality graphics and/or video, digital video disk (DVD) players and set-top boxes (abstract, lines 14-16)". Therefore, it would have been obvious to modify BUCKELEW et al by VAINSENCHER because both inventions

share similar technological environments corresponding to graphics and video processings in single chip computer systems.

9. As per claim 13, BUCKELEW et al as modified meet limitations for claim 14, however, BUCKELEW et al does not explicitly teach the limitation of claim 12. VAINSENCHERI suggest, "..wherein said processor reads compressed texture data from said first storage device, said data decompression circuit decompresses said read compressed texture data, and said processor stores said decompressed texture data in said texture buffer (figure 2, column 4, line 54-column 5, line 14, please note element 206-MPEG Coprocessor for decompression/compression means); reading said compressed texture data from said storage device and decompressing said compressed texture data in a texture buffer (figure 2, column 4, line 54-column 5, line 14, please note element 206-MPEG Coprocessor for decompression/compression means).

It would have been obvious to one skilled in the art at the time of the invention to utilize **multimedia computer chip system 200** of figure 2 as a processor including the MPEG Coprocessor of decompression means with the graphic engine means (figure 1, including elements 124-graphics engine integrated into a single chip (integrate a texture processor and graphics engine) and element 110-a set of dual resolver chips combine to bear similar results to a graphics engine contained within a single chip, including electrically coupled components 114-texture buffer and 116-frame buffer) of BUCKELEW et al because both inventions were designed for single chip computer

systems. **Advantages of single chip computer systems** by VAINSECHER are at least as follows, "..highly integrated, single chip computer system.(abstract, line 1), as well as adding a further advantage of "[T]he single chip computer system is particularly suitable for video game consoles having high quality graphics and/or video, digital video disk (DVD) players and set-top boxes (abstract, lines 14-16)". Therefore, it would have been obvious to modify BUCKELEW et al by VAINSENCHER because both inventions share similar technological environments corresponding to graphics and video processings in single chip computer systems.

10. As per claim 16, BUCKELEW et al as modified meet limitations for claim 14. BUCKELEW et al suggest, "..wherein said processor includes a FIFO storage device which temporarily stores said read compressed texture data (column 11, lines 52-column 12, line 27). It would have been obvious to one skilled in the art at the time of the invention to utilize **multimedia computer chip system 200** of figure 2 as a processor including the MPEG Coprocessor of decompression means with the graphic engine means (figure 1, including elements 124-graphics engine integrated into a single chip (integrate a texture processor and graphics engine) and element 110-a set of dual resolver chips combine to bear similar results to a graphics engine contained within a single chip, including electrically coupled components 114-texture buffer and 116-frame buffer) of BUCKELEW et al because both inventions were designed for single chip computer systems. **Advantages of single chip computer systems** by VAINSECHER are at least as follows, "..highly integrated, single chip computer system.(abstract, line 1),

as well as adding a further advantage of "[T]he single chip computer system is particularly suitable for video game consoles having high quality graphics and/or video, digital video disk (DVD) players and set-top boxes (abstract, lines 14-16)". Therefore, it would have been obvious to modify BUCKELEW et al by VAINSENCHER because both inventions share similar technological environments corresponding to graphics and video processings in single chip computer systems.

11. As per claim 17, BUCKELEW et al as modified meet limitations for claim 16. BUCKELEW et al suggest, "..wherein said data decompression circuit receives said compressed texture data from said FIFO storage device" (column 11, lines 52-column 12, line 27). It would have been obvious to one skilled in the art at the time of the invention to utilize **multimedia computer chip system 200** of figure 2 as a processor including the MPEG Coprocessor of decompression means with the graphic engine means (figure 1, including elements 124-graphics engine integrated into a single chip (integrate a texture processor and graphics engine) and element 110-a set of dual resolver chips combine to bear similar results to a graphics engine contained within a single chip, including electrically coupled components 114-texture buffer and 116-frame buffer) of BUCKELEW et al because both inventions were designed for single chip computer systems. **Advantages of single chip computer systems** by VAINSECHER are at least as follows, "..highly integrated, single chip computer system (abstract, line 1), as well as adding a further advantage of "[T]he single chip computer system is particularly suitable for video game consoles having high quality graphics and/or video,

digital video disk (DVD) players and set-top boxes (abstract, lines 14-16)". Therefore, it would have been obvious to modify BUCKELEW et al by VAINSENCHER because both inventions share similar technological environments corresponding to graphics and video processings in single chip computer systems.

12. As per claim 18. BUCKELEW et al as modified meet limitations of claim 13, further, BUCKELEW et al suggest, "... wherein said processor includes a palette transformation circuit-RAMDAC 112 of Frame Buffer 116 (column 13, lines 44-60)", corresponds to recited limitations of claim 19, "..transformation circuit performing palette transformation of said decompressed texture data". It would have been obvious to one skilled in the art at the time of the invention to utilize **multimedia computer chip system 200** of figure 2 as a processor including the MPEG Coprocessor of decompression means with the graphic engine means (figure 1, including elements 124-graphics engine integrated into a single chip (integrate a texture processor and graphics engine) and element 110-a set of dual resolver chips combine to bear similar results to a graphics engine contained within a single chip, including electrically coupled components 114-texture buffer and 116-frame buffer) of BUCKELEW et al because both inventions were designed for single chip computer systems. **Advantages of single chip computer systems** by VAINSECHER are at least as follows, "..highly integrated, single chip computer system (abstract, line 1), as well as adding a further advantage of "[T]he single chip computer system is particularly suitable for video game consoles having high quality graphics and/or video, digital video disk (DVD) players and

set-top boxes (abstract, lines 14-16)". Therefore, it would have been obvious to modify BUCKELEW et al by VAINSENCHER because both inventions share similar technological environments corresponding to graphics and video processings in single chip computer systems.

13. As per claim 19. BUCKELEW et al as modified meet limitations for claim 13. BUCKELEW et al does not expressly teach limitations of claim 19. VAINSENCHER teaches "The processing of the display controller 238 includes horizontal and vertical filtering as well as color space conversions (column 5, lines 54-57)" corresponding to recited limitations of claim 19, "..wherein said processor includes a mip map generation circuit, said mip map generation circuit generating a mip map of said decompressed texture data (column 5, lines 45-64).

It would have been obvious to one skilled in the art at the time of the invention to utilize **multimedia computer chip system 200** of figure 2 as a processor including the MPEG Coprocessor of decompression means with the graphic engine means (figure 1, including elements 124-graphics engine integrated into a single chip (integrate a texture processor and graphics engine) and element 110-a set of dual resolver chips combine to bear similar results to a graphics engine contained within a single chip, including electrically coupled components 114-texture buffer and 116-frame buffer) of BUCKELEW et al because both inventions were designed for single chip computer systems. **Advantages of single chip computer systems** by VAINSECHER are at least as follows, "..highly integrated, single chip computer system (abstract, line 1), as well

as adding a further advantage of "[T]he single chip computer system is particularly suitable for video game consoles having high quality graphics and/or video, digital video disk (DVD) players and set-top boxes (abstract, lines 14-16)". Therefore, it would have been obvious to modify BUCKELEW et al by VAINSENCHER because both inventions share similar technological environments corresponding to graphics and video processings in single chip computer systems.

14. As per claim 20, BUCKELEW et al as modified meet limitations for claim 14. BUCKELEW et al suggest," wherein said texture data in said first storage device is compressed (figure 1, element 128 serves as a port transferring texture data to texture memory, element 114)". It would have been obvious to one skilled in the art at the time of the invention to utilize **multimedia computer chip system 200** of figure 2 as a processor including the MPEG Coprocessor of decompression means with the graphic engine means (figure 1, including elements 124-graphics engine integrated into a single chip (integrate a texture processor and graphics engine) and element 110-a set of dual resolver chips combine to bear similar results to a graphics engine contained within a single chip, including electrically coupled components 114-texture buffer and 116-frame buffer) of BUCKELEW et al because both inventions were designed for single chip computer systems. **Advantages of single chip computer systems** by VAINSECHER are at least as follows, "..highly integrated, single chip computer system (abstract, line 1), as well as adding a further advantage of "[T]he single chip computer system is particularly suitable for video game consoles having high quality graphics and/or video,

digital video disk (DVD) players and set-top boxes (abstract, lines 14-16)". Therefore, it would have been obvious to modify BUCKELEW et al by VAINSENCHER because both inventions share similar technological environments corresponding to graphics and video processings in single chip computer systems.

It would have been obvious to one skilled in the art at the time of the invention to utilize **multimedia computer chip system 200** of figure 2 as a processor including the MPEG Coprocessor of decompression means with the graphic engine means (figure 1, including elements 124-graphics engine integrated into a single chip (integrate a texture processor and graphics engine) and element 110-a set of dual resolver chips combine to bear similar results to a graphics engine contained within a single chip, including electrically coupled components 114-texture buffer and 116-frame buffer) of BUCKELEW et al because both inventions were designed for single chip computer systems. **Advantages of single chip computer systems** by VAINSECHER are at least as follows, "..highly integrated, single chip computer system.(abstract, line 1), as well as adding a further advantage of "[T]he single chip computer system is particularly suitable for video game consoles having high quality graphics and/or video, digital video disk (DVD) players and set-top boxes (abstract, lines 14-16)". Therefore, it would have been obvious to modify BUCKELEW et al by VAINSENCHER because both inventions share similar technological environments corresponding to graphics and video processings in single chip computer systems.

15. As per claim 22, BUCKELEW et al as modified meet limitations for claim 23. BUCKELEW et al does not expressly teach limitations of claim 22. VAINSENCHER (figure 2, column 4, line 54-column 5, line 14, please note element 206-MPEG Coprocessor for decompression/compression means) suggests, "further comprising the step of converting said decompressed texture data to image data, and storing said image data in a frame buffer.

It would have been obvious to one skilled in the art at the time of the invention to utilize **multimedia computer chip system 200** of figure 2 as a processor including the MPEG Coprocessor of decompression means with the graphic engine means (figure 1, including elements 124-graphics engine integrated into a single chip (integrate a texture processor and graphics engine) and element 110-a set of dual resolver chips combine to bear similar results to a graphics engine contained within a single chip, including electrically coupled components 114-texture buffer and 116-frame buffer) of BUCKELEW et al because both inventions were designed for single chip computer systems. **Advantages of single chip computer systems** by VAINSECHER are at least as follows, "..highly integrated, single chip computer system (abstract, line 1), as well as adding a further advantage of "[T]he single chip computer system is particularly suitable for video game consoles having high quality graphics and/or video, digital video disk (DVD) players and set-top boxes (abstract, lines 14-16)". Therefore, it would have been obvious to modify BUCKELEW et al by VAINSENCHER because both inventions share similar technological environments corresponding to graphics and video processings in single chip computer systems.

16. As per claim 24, BUCKELEW et al as modified meet limitations for claim 23. BUCKELEW et al discloses wherein said processor includes a palette transformation circuit-RAMDAC 112 of Frame Buffer 116 (column 13, lines 44-60)", corresponds to recited limitations of claim 19, "...further comprising the step of performing palette conversion of said processor faster than said transferring data between said storage device and said processor."

It would have been obvious to one skilled in the art at the time of the invention to utilize **multimedia computer chip system 200** of figure 2 as a processor including the MPEG Coprocessor of decompression means with the graphic engine means (figure 1, including elements 124-graphics engine integrated into a single chip (integrate a texture processor and graphics engine) and element 110-a set of dual resolver chips combine to bear similar results to a graphics engine contained within a single chip, including electrically coupled components 114-texture buffer and 116-frame buffer) of BUCKELEW et al because both inventions were designed for single chip computer systems. **Advantages of single chip computer systems** by VAINSECHER are at least as follows, "..highly integrated, single chip computer system (abstract, line 1), as well as adding a further advantage of "[T]he single chip computer system is particularly suitable for video game consoles having high quality graphics and/or video, digital video disk (DVD) players and set-top boxes (abstract, lines 14-16)". Therefore, it would have been obvious to modify BUCKELEW et al by VAINSENCHER because both inventions

share similar technological environments corresponding to graphics and video processings in single chip computer systems.

17. As per claim 25, BUCKELEW et al as modified meet limitations for claim 23. BUCKELEW et al does not expressly teach limitations of claim 25.

VAINSENCHER teaches "The processing of the display controller 238 includes horizontal and vertical filtering as well as color space conversions (column 5, lines 54-57)" corresponds to recited limitations of claim 25, "...further comprising the step of generating a mip map of said compressed texture data prior to said step of storing said decompressed texture data (column 5, lines 45-64)".

It would have been obvious to one skilled in the art at the time of the invention to utilize **multimedia computer chip system 200** of figure 2 as a processor including the MPEG Coprocessor of decompression means with the graphic engine means (figure 1, including elements 124-graphics engine integrated into a single chip (integrate a texture processor and graphics engine) and element 110-a set of dual resolver chips combine to bear similar results to a graphics engine contained within a single chip, including electrically coupled components 114-texture buffer and 116-frame buffer) of BUCKELEW et al because both inventions were designed for single chip computer systems. **Advantages of single chip computer systems** by VAINSECHER are at least as follows, "..highly integrated, single chip computer system (abstract, line 1), as well as adding a further advantage of "[T]he single chip computer system is particularly suitable for video game consoles having high quality graphics and/or video, digital video

disk (DVD) players and set-top boxes (abstract, lines 14-16)". Therefore, it would have been obvious to modify BUCKELEW et al by VAINSENCHER because both inventions share similar technological environments corresponding to graphics and video processings in single chip computer systems.

18. As per claim 26. BUCKELEW et al as modified meet limitations for claim 23. BUCKELEW et al does not expressly teach limitations of claim 26. VAINSENCHER teaches "The processing of the display controller 238 includes horizontal and vertical filtering as well as color space conversions (column 5, lines 54-57)" corresponds to recited limitations of claim 25, "..further comprising the step of generating a mip map of said compressed texture data prior to said step of storing said decompressed texture data (column 5, lines 45-64)".

It would have been obvious to one skilled in the art at the time of the invention to utilize **multimedia computer chip system 200** of figure 2 as a processor including the MPEG Coprocessor of decompression means with the graphic engine means (figure 1, including elements 124-graphics engine integrated into a single chip (integrate a texture processor and graphics engine) and element 110-a set of dual resolver chips combine to bear similar results to a graphics engine contained within a single chip, including electrically coupled components 114-texture buffer and 116-frame buffer) of BUCKELEW et al because both inventions were designed for single chip computer systems. **Advantages of single chip computer systems** by VAINSECHER are at least as follows, "..highly integrated, single chip computer system (abstract, line 1), as well

as adding a further advantage of "[T]he single chip computer system is particularly suitable for video game consoles having high quality graphics and/or video, digital video disk (DVD) players and set-top boxes (abstract, lines 14-16)". Therefore, it would have been obvious to modify BUCKELEW et al by VAINSENCHER because both inventions share similar technological environments corresponding to graphics and video processings in single chip computer systems.

19. As per claim 27, BUCKELEW et al as modified meet limitations for claim 23, BUCKELEW et al suggest, "further comprising a frame buffer, wherein said processor stores image data in said frame buffer (column 2, lines 23-46, 47-64 represent two separate embodiments and column 3, line 62-column 4, line 15).

It would have been obvious to one skilled in the art at the time of the invention to utilize **multimedia computer chip system 200** of figure 2 as a processor including the MPEG Coprocessor of decompression means with the graphic engine means (figure 1, including elements 124-graphics engine integrated into a single chip (integrate a texture processor and graphics engine) and element 110-a set of dual resolver chips combine to bear similar results to a graphics engine contained within a single chip, including electrically coupled components 114-texture buffer and 116-frame buffer) of BUCKELEW et al because both inventions were designed for single chip computer systems. **Advantages of single chip computer systems** by VAINSECHER are at least as follows, "..highly integrated, single chip computer system (abstract, line 1), as well as adding a further advantage of "[T]he single chip computer system is particularly

suitable for video game consoles having high quality graphics and/or video, digital video disk (DVD) players and set-top boxes (abstract, lines 14-16)". Therefore, it would have been obvious to modify BUCKELEW et al by VAINSENCHER because both inventions share similar technological environments corresponding to graphics and video processings in single chip computer systems.

20. As per claim 28, BUCKELEW et al as modified meet limitations for claim 15, however, BUCKELEW et al does not explicitly teach the limitation of claim 28. VAINSENCHER suggest,"..wherein said processor reads decompressed texture data contained in said buffer and performs image processing of said decompressed texture data for conversion to image data (figure 2, column 4, line 54-column 5, line 14, please note element 206-MPEG Coprocessor for decompression/compression means).

It would have been obvious to one skilled in the art at the time of the invention to utilize **multimedia computer chip system 200** of figure 2 as a processor including the MPEG Coprocessor of decompression means with the graphic engine means (figure 1, including elements 124-graphics engine integrated into a single chip (integrate a texture processor and graphics engine) and element 110-a set of dual resolver chips combine to bear similar results to a graphics engine contained within a single chip, including electrically coupled components 114-texture buffer and 116-frame buffer) of BUCKELEW et al because both inventions were designed for single chip computer systems. **Advantages of single chip computer systems** by VAINSECHER are at least as follows, "..highly integrated, single chip computer system (abstract, line 1), as well

as adding a further advantage of "[T]he single chip computer system is particularly suitable for video game consoles having high quality graphics and/or video, digital video disk (DVD) players and set-top boxes (abstract, lines 14-16)". Therefore, it would have been obvious to modify BUCKELEW et al by VAINSENCHER because both inventions share similar technological environments corresponding to graphics and video processings in single chip computer systems.

21. As per claim 29, BUCKELEW et al as modified meet limitations for claim 15, however, BUCKELEW et al does not explicitly teach the limitation of claim 29. VAINSENCHER suggest,"wherein said processor reads compressed texture data from said first storage device, said data decompression circuit decompresses said read compressed texture data, and said processor stores said decompressed texture data in said texture buffer (figure 2, column 4, line 54-column 5, line 14, please note element 206-MPEG Coprocessor for decompression/compression means).

It would have been obvious to one skilled in the art at the time of the invention to utilize **multimedia computer chip system 200** of figure 2 as a processor including the MPEG Coprocessor of decompression means with the graphic engine means (figure 1, including elements 124-graphics engine integrated into a single chip (integrate a texture processor and graphics engine) and element 110-a set of dual resolver chips combine to bear similar results to a graphics engine contained within a single chip, including electrically coupled components 114-texture buffer and 116-frame buffer) of BUCKELEW et al because both inventions were designed for single chip computer

systems. **Advantages of single chip computer systems** by VAINSECHER are at least as follows, "..highly integrated, single chip computer system (abstract, line 1), as well as adding a further advantage of "[T]he single chip computer system is particularly suitable for video game consoles having high quality graphics and/or video, digital video disk (DVD) players and set-top boxes (abstract, lines 14-16)". Therefore, it would have been obvious to modify BUCKELEW et al by VAINSENCHER because both inventions share similar technological environments corresponding to graphics and video processings in single chip computer systems.

22. As per claim 30, BUCKELEW et al as modified meet limitations for claim 29. BUCKELEW et al suggest," wherein said processor includes a FIFO storage device which temporarily stores said read compressed texture data (column 11, lines 52-column 12, line 27).

It would have been obvious to one skilled in the art at the time of the invention to utilize **multimedia computer chip system 200** of figure 2 as a processor including the MPEG Coprocessor of decompression means with the graphic engine means (figure 1, including elements 124-graphics engine integrated into a single chip (integrate a texture processor and graphics engine) and element 110-a set of dual resolver chips combine to bear similar results to a graphics engine contained within a single chip, including electrically coupled components 114-texture buffer and 116-frame buffer) of BUCKELEW et al because both inventions were designed for single chip computer systems. **Advantages of single chip computer systems** by VAINSECHER are at

least as follows, "..highly integrated, single chip computer system.(abstract, line 1), as well as adding a further advantage of "[T]he single chip computer system is particularly suitable for video game consoles having high quality graphics and/or video, digital video disk (DVD) players and set-top boxes (abstract, lines 14-16)". Therefore, it would have been obvious to modify BUCKELEW et al by VAINSENCHER because both inventions share similar technological environments corresponding to graphics and video processings in single chip computer systems.

23. As per claim 31, BUCKELEW et al as modified meet limitations for claim 30. BUCKELEW et al suggest, "..wherein said data decompression circuit receives said read compressed texture data from said FIFO storage device (column 11, lines 52-column 12, line 27).

It would have been obvious to one skilled in the art at the time of the invention to utilize **multimedia computer chip system 200** of figure 2 as a processor including the MPEG Coprocessor of decompression means with the graphic engine means (figure 1, including elements 124-graphics engine integrated into a single chip (integrate a texture processor and graphics engine) and element 110-a set of dual resolver chips combine to bear similar results to a graphics engine contained within a single chip, including electrically coupled components 114-texture buffer and 116-frame buffer) of BUCKELEW et al because both inventions were designed for single chip computer systems. **Advantages of single chip computer systems** by VAINSECHER are at least as follows, "..highly integrated, single chip computer system.(abstract, line 1), as well

as adding a further advantage of "[T]he single chip computer system is particularly suitable for video game consoles having high quality graphics and/or video, digital video disk (DVD) players and set-top boxes (abstract, lines 14-16)". Therefore, it would have been obvious to modify BUCKELEW et al by VAINSENCHER because both inventions share similar technological environments corresponding to graphics and video processings in single chip computer systems.

24. As per claim 32. BUCKELEW et al as modified meet limitations for claim 30. BUCKELEW et al suggest, wherein said processor includes a palette transformation circuit-RAMDAC 112 of Frame Buffer 116 (column 13, lines 44-60)", corresponds to recited limitations of claim 19, "..transformation circuit performing palette transformation of said decompressed texture data".

It would have been obvious to one skilled in the art at the time of the invention to utilize **multimedia computer chip system 200** of figure 2 as a processor including the MPEG Coprocessor of decompression means with the graphic engine means (figure 1, including elements 124-graphics engine integrated into a single chip (integrate a texture processor and graphics engine) and element 110-a set of dual resolver chips combine to bear similar results to a graphics engine contained within a single chip, including electrically coupled components 114-texture buffer and 116-frame buffer) of BUCKELEW et al because both inventions were designed for single chip computer systems. **Advantages of single chip computer systems** by VAINSECHER are at least as follows, "..highly integrated, single chip computer system (abstract, line 1), as well

as adding a further advantage of "[T]he single chip computer system is particularly suitable for video game consoles having high quality graphics and/or video, digital video disk (DVD) players and set-top boxes (abstract, lines 14-16)". Therefore, it would have been obvious to modify BUCKELEW et al by VAINSENCHER because both inventions share similar technological environments corresponding to graphics and video processings in single chip computer systems.

25. As per claim 33, BUCKELEW et al as modified meet limitations for claim 29, however, BUCKELEW et al does not explicitly teach the limitation of claim 33. VAINSENCHER teaches "The processing of the display controller 238 includes horizontal and vertical filtering as well as color space conversions (column 5, lines 54-57)" corresponding to recited limitations of claim 19, "..wherein said processor includes a mip map generation circuit, said mip map generation circuit generating a mip map of said decompressed texture data (column 5, lines 45-64).

It would have been obvious to one skilled in the art at the time of the invention to utilize **multimedia computer chip system 200** of figure 2 as a processor including the MPEG Coprocessor of decompression means with the graphic engine means (figure 1, including elements 124-graphics engine integrated into a single chip (integrate a texture processor and graphics engine) and element 110-a set of dual resolver chips combine to bear similar results to a graphics engine contained within a single chip, including electrically coupled components 114-texture buffer and 116-frame buffer) of BUCKELEW et al because both inventions were designed for single chip computer

systems. **Advantages of single chip computer systems** by VAINSECHER are at least as follows, "..highly integrated, single chip computer system.(abstract, line 1), as well as adding a further advantage of "[T]he single chip computer system is particularly suitable for video game consoles having high quality graphics and/or video, digital video disk (DVD) players and set-top boxes (abstract, lines 14-16)". Therefore, it would have been obvious to modify BUCKELEW et al by VAINSENCHER because both inventions share similar technological environments corresponding to graphics and video processings in single chip computer systems.

26. As per claim 34, BUCKELEW et al as modified meet limitations for claim 29, however, BUCKELEW et al does not explicitly teach the limitation of claim 33. VAINSENCHER suggest, "..wherein said texture data in said first storage device is compressed (figure 2, column 4, line 54-column 5, line 14, please note element 206-MPEG Coprocessor for decompression means).

It would have been obvious to one skilled in the art at the time of the invention to utilize **multimedia computer chip system 200** of figure 2 as a processor including the MPEG Coprocessor of decompression means with the graphic engine means (figure 1, including elements 124-graphics engine integrated into a single chip (integrate a texture processor and graphics engine) and element 110-a set of dual resolver chips combine to bear similar results to a graphics engine contained within a single chip, including electrically coupled components 114-texture buffer and 116-frame buffer) of BUCKELEW et al because both inventions were designed for single chip computer

systems. **Advantages of single chip computer systems** by VAINSECHER are at least as follows, "..highly integrated, single chip computer system.(abstract, line 1), as well as adding a further advantage of "[T]he single chip computer system is particularly suitable for video game consoles having high quality graphics and/or video, digital video disk (DVD) players and set-top boxes (abstract, lines 14-16)". Therefore, it would have been obvious to modify BUCKELEW et al by VAINSENCHER because both inventions share similar technological environments corresponding to graphics and video processings in single chip computer systems.

Conclusion

27. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. HAMADDANI et al, US Patent No. 5,845,083 teach an MPEG encoding/decoding/compression/decompression of texture data for multimedia applications (column 8, lines 12-32 and figures 3 and 6). KENWORTHY et al, US Patent No. 5,808,617 teach a graphics rendering system including compression/decompression of texture data.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ANTHONY J BLACKMAN whose telephone number is 703-305-0833. The examiner can normally be reached on FLEX SCHEDULE.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, MATTHEW BELLA can be reached on 703-308-6829. The fax phone

numbers for the organization where this application or proceeding is assigned are 703-872-9314 for regular communications and 703-746-5731 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

ANTHONY J BLACKMAN
Examiner
Art Unit 2676

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February 6, 2004

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